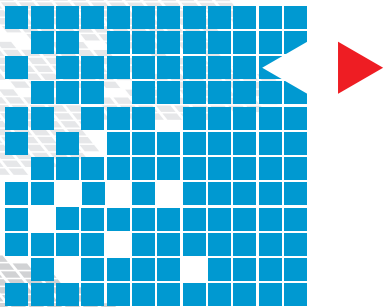
Program

CATRENE
Design Technology Conference

jointly organized



edaWorkshop **11**

www.edacentrum.de/edaworkshop

Dresden (Germany), May 10 – 12, 2011

About edaWorkshop and CATRENE DTC

The edaWorkshop is the premier German EDA event for the publication and discussion of application-oriented EDA research findings. The mix of representatives from industry and academic research creates ideal opportunities for a professional exchange of ideas on a scientific basis. The dialog can pave the way for industry to benefit from research results.

The edaWorkshop is also the primary platform for presenting and exchanging solution approaches and results of EDA projects funded by the BMBF (Federal Ministry of Education and Research). It promotes communication between EDA experts and public authorities, and supports the dissemination of the results of publicly-funded projects.

edaWorkshop **11**

The edaWorkshop is organized jointly by the edacentrum and BMBF, DLR and the GI/GMM/ITG RSS Steering Group for "Computer-aided Circuit and System Design".

Like in 2009, the edaWorkshop will co-locate and share a common day – including keynotes, sessions and the social event – with the annual CATRENE Design Technology Conference (CATRENE DTC), successor of the MEDEA+ DAC. The CATRENE DTC is the meeting point of Europe's scientists and experts in application-oriented design. Leading research and development in design automation has been supported by CATRENE and EUREKA member states during the past ten years. Both events are attracting European experts in industry and academia and consequently the organizers decided this year to co-locate the workshop and the conference.

The three days event is a balanced combination of information and communication. It not only offers a wide range of discussions on specialized subjects and EDA research projects, but also provides several networking opportunities. This is supported by a comprehensive poster exhibition, where demonstrations and prototypes will also be presented.

Looking forward to seeing you in Dresden!

Prof. Dr. W. Rosenstiel
Prof. Dr. E. Barke
General Chairs

The edaWorkshop and CATRENE DTC – Catalyst of EDA Research

The design of integrated circuits and systems places enormous demands on R&D engineers and the design methods and tools that they use. It requires the efficient and manufacturing-aware development of safe, economical, robust and reliable systems of high complexity with very small structures, and the design of analog and mixed-signal circuits.

In order to stimulate EDA research activities to deal with these challenges, the BMBF (Federal Ministry of Education and Research) has established as part of its research program IKT 2020 an R&D program on design platforms for complex applied systems and circuits. In these IKT 2020 EDA-projects industry and research join forces with the public authorities to support those areas that are vital for the competitiveness of the German industry. There are five application fields with a potentially high added value, and with considerable potential for job creation: automotive/mobility, mechanical engineering/automation, health/medicine, logistics/services and energy/environment.

In many cases the projects on these application fields include European-wide collaboration, they are contributing to the research program of CATRENE. IKT 2020 and CATRENE complement each other and offer a lot of valuable synergies.

This event is a central platform for exchanging information concerning the approaches and results of projects from IKT 2020 and CATRENE as well. People involved in the projects are invited to present their results by means of talks and posters. At the heart of these presentations will be the relevance of the applications to topics affecting society (as defined in IKT 2020 and CATRENE White Book, part B). As second essential part of the event, the project presentations will be supplemented by a selection of peer-reviewed scientific papers on R&D results.

This year the edaWorkshop is jointly organized with the CATRENE Design Technology Conference (CATRENE DTC). Hence it provides a comprehensive overview of latest algorithms and tools, emerging technologies, key CATRENE and IKT 2020 projects, and advanced research in application-oriented SoC design automation in Europe. The joint event consists of a CATRENE DTC day (May 10), an edaWorkshop day (May 12), and a joint day common to both (May 11).

For more information on CATRENE see www.catrene.org

Federal Ministry of Education and Research

edacentrum

ITG

GMM

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EUREKA

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Bastiaan de Groot: "Real-world Applications of Smart Environments in the Home"

Abstract:
Examples and future visions of Smart Environments in the home have been around for a long time, but despite our fast advancement in reducing chip cost, power usage and processing power, only a fraction of the envisioned use cases have been realized. This is mainly caused by the high level of integration on a semantic level that is needed to realize many of the use cases and the absence of applications that could justify the investments in a backbone infrastructure for the home. This is currently changing rapidly, with the increasing societal cost of energy and an aging population, there suddenly is the societal need that justifies the installation of the needed infrastructure in the home. With emergence of standards like Zigbee and Continua we are also well on our way to solve the problem of semantic standardization for these domains.

The interesting question that remains is how the end-user and other stakeholders will react to these developments, with the pressure to change mainly being driven by a societal need and not by an end-user insight, these developments are met with great skepticism by the end-users (as we can see with the introduction of for example the smart meter). The major question will be how to involve the end-user in such a way that he will embrace this type of solutions and this is (usually) not the case when the only benefit is financial. Only if the solutions add true value to the lives of the consumers they will fully embrace the solutions developed, something which is often overlooked in many societal driven developments. In this talk an outline will be given of end-user driven developments in this field from the perspective of Philips Research.

Keynote: "More than Moore - Challenges and Opportunities for Europe"

For further information on this keynote see the online program at www.edacentrum.de/edaworkshop.

Curriculum Vitae:
Bastiaan de Groot is a System Designer at Philips Research. Before joining Philips Research he worked for Philips Applied Technologies; realizing first-of-a-kind products for both Philips and non-Philips customers. His focus is on creating new market propositions based on insights from end-user driven research, strategic business objectives and state of the art technologies. He received a Master of Science in Artificial Intelligence (Cum Laude) from the University of Amsterdam in 2008, completing his graduation work at Microsoft Research, Cambridge, UK.

Gerd Teepe, Philippe Magarshack: "Gaining 10x in Power Efficiency in the Next Decade in Consumer Products"

Abstract:
Analog/RF design is becoming digital, through accurate CAD modeling of RF effects, and compensation in digital. At the same time, energy-efficient Digital is becoming Analog, thanks to elaborate CAD-enabled design techniques like well-biasing, power-switches, over-/under-voltage, etc. In Analog/RF, improving the energy efficiency of consumer systems will be based on sensing continuously the system environment and tailoring the emitted power dynamically. Similarly in Digital, very-fine-grain closed-loop Dynamic-Voltage-Frequency-Scaling (DVFS) will enable to consume power only when and where required. Concurrently, heterogeneous co-design CAD methods will allow a holistic approach to energy efficiency, taking into consideration not only the IC with its system design architecture, but also its packaging and power source, and possibly the antenna.

Finally, a tailored advanced CMOS process will provide tuned transistors and passive components to enable the digital and analog design solutions needed, in conjunction with TSVs enabling optimized heterogeneous 3D stacking capabilities. A new generation of EDA tools, providing a holistic view of the system, will enable the complete system optimization and a 10x power efficiency gain.

In Europe, the Grenoble-Dresden Clusters are uniquely positioned to address the above challenges with a complete set of world-class industrial and academic research facilities in advanced CMOS, 3D-stacking, design, system architectures and EDA.

Curriculum Vitae Gerd Teepe:
Gerd Teepe is director of Dresden Design Enablement of GLOBALFOUNDRIES. He graduated from the RWTH Aachen University (Dipl. 1982, PhD. 1986). He then worked on fault tolerant microprocessors at the NEC-Central-Research-Laboratories, Tokyo, Japan. For Motorola-Semiconductors in Europe, Teepe held various engineering and management positions in design, marketing and product-operations. Gerd Teepe joined AMD in Dresden in 2004 and is part of GLOBALFOUNDRIES since its foundation in 2009.

Curriculum Vitae Philippe Magarshack:
Philippe Magarshack is Technology Group Vice-President and Central CAD & Design Solutions General Manager at STMicroelectronics in Crolles, France. He started his career at AT&T Bell Labs in Murray Hill, NJ, in 1984, as a designer for the first 32bit microprocessor family. In 1989 in joined Thomson-CSF in Grenoble, and in 1994, he joined the Central R&D group at STMicroelectronics in Crolles. Magarshack now oversees ST's EDA and libraries strategy, enabling products in advanced CMOS and derivatives, and Smart Power.

Lars Hedrich: "Design and Verification of Dependable Analog Systems"

Abstract:
Today's deep submicron technologies enable the implementation of multi core mixed-signal systems on chip with a reasonable part of analog blocks. These blocks have to be designed and verified in very short design cycles. On the other hand, failures in analog parts are costly, as they are not easily removed by reloading a firmware. In many cases analog circuits could inhibit the proper function of the whole chip due to their central role in clock generators or power supplies. Additionally, real push button solutions for analog synthesis and complete verification are not available resulting in high efforts in product development.

The situation is getting even worse with the upcoming aging and degradation effects. Therewith, the analog transistor parameters will not only vary with the fabrication process, they will also vary over circuit lifetime. The degradation is additionally signal dependent, turning the estimation of failure rates and lifetime into a difficult process.

The talk will give an overview about EDA concepts for tackling the verification problem in different ways. The presented concepts range from extended reliability simulation techniques to user-oriented formal verification techniques for analog systems. The latter attracts more interest since the verification of hybrid systems evolve rapidly enabling a high-level proof of mixed-signal systems. This is accompanied by some languages for formulating analog specifications.

Having these methods available, experimental design principles for dependable analog blocks as part of large systems on chip will be discussed. A possible implementation uses self organizing and self healing features to harden analog functionality at the cost of circuit size.

Curriculum Vitae:
Lars Hedrich is a full professor at the Institute of Computer Science, University of Frankfurt, where he is head of the design methodology group. He was born in Hanover, Germany, in 1966 and graduated (Dipl.-Ing.) in electrical engineering at the University of Hanover in 1992. In 1997, he received the Ph.D. degree and became an assistant professor at the same university in 2002, before he moved to Frankfurt in 2004. His research interests include several areas of analog design automation: symbolic analysis of linear and nonlinear circuits, behavioral modeling, automatic circuit synthesis, formal verification and robust design.

edaWorkshop11 and CATRENE DTC Topics

System Level and Hardware/Software Design of Embedded Systems

- Specification- and Model-based Design
- Architectural Synthesis and Optmization
- Advanced Architectures (ASIPs, SoCs, MPSoCs, NoC, SiPs and Reconfigurable Architectures)
- Transaction Level Modeling and Simulation
- Development and Optimization of Hardware-dependent Software

Design and Verification

- Formal Verification
- Statistical Timing Analysis and Variability
- Low Power Design, Analysis and Optimization
- Logic- and Technology-dependent Synthesis for Nanometer Circuits
- Physical Design and Verification
- Simulation Acceleration and Rapid Prototyping
- Productivity and Efficiency of Design

Analog- and Mixed-Signal Design

- Design Automation for Analog Circuits
- Synthesis, Simulation and Verification
- RF Circuits, Smart Power Circuits
- Model Generation
- Parasitics and Interconnects
- Signal Integrity and EMC

More than Moore

- 3D Design, Packaging and SiP
- Design for Integration of Multi-Domain components
- Energy Efficient Design
- Analysis and Optimization of Performance and Power
- Cyber-Physical Systems

Reliability, Robustness and Test

- Design for Reliability and Robustness
- Modeling of Aging Effects
- Design Centering and Yield Optimization (DfM)
- Fault-tolerant and Self-healing System Design
- System Test and Production Test
- Delay Test and Defect-oriented Test
- BIST and Design for Testability
- Test Generation, Diagnosis and Fault Modeling
- Test of Regular Structures

Registration

The participation fee includes 3 days conference, 3x lunch, 2x dinner, conference beverages and conference documents. This is an all-inclusive package. Items are not available separately.

Registration	until April 10, 2011	after April 10, 2011
Participation fee (All prices plus 19 % VAT)	EUR 335,–	EUR 395,–

Payment is possible by bank transfer or credit card: MasterCard, VISA or AMEX.
Registration deadline is on May 2, 2011.

To register choose the registration online (http://www.edacentrum.de/edaworkshop/online-registration) or fax the registration form to +49 511 762-19695.

For questions please contact: Ms. Maren Sperber, fon +49 511 762-19699, sperber@edacentrum.de

Cancellation (only by written request) is possible free of charge until April 25, 2011. Until May 2, 2011, half of the participation fee is retained. After this date the entire participation fee is due.
A replacement for the registered participant with the same affiliation is possible at any time.

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Tuesday, May 10, 2011

	Keynote Moderator: E. Barke (edacentrum)
9:15	**Welcome** A. Brüning (Silicon Saxony)
9:30	**More than Moore - Challenges and Opportunities for Europe** M. Brillouet (LETI) (to be confirmed)
10:00	**Real-world Applications of Smart Environments in the Home** B. de Groot (Philips)
10:30	**Coffee Break**
	Technical Session: Healthcare Moderator: P. Merkus (Philips)
11:00	**THOR: Striking Technologies for Power** M. van Helvoort (Philips)
11:35	**CSI: Central Nervous System's Multi Modal Imaging** R. Zafalon (STMicroelectronics Italy)
12:00	**MAS: Mobile Ambient Assisted Living** O. Vermesan (SINTEF)
12:25	**Q&A** P. Merkus (Philips)
12:30	**Lunch**
	Technical Session: System Design Methodologies Moderator: F. Petrot (TIMA)
14:00	**Multimedia Box to Home System** D. Henoff (STMicroelectronics)
14:35	**Hardware Dependent Software Solutions for SoC Design** E. de Kock (NXP)
15:00	**An Approach toward Accurately Timed TLM+ for Embedded System Models** K. Lu, D. Müller-Gritschneder, W. Ecker, V. Esen, M. Velten, U. Schlichtmann (Infineon, TU München)
15:25	**Q&A** F. Petrot (TIMA)
15:30	**Coffee Break**
	Technical Session: Multicore Architecture Moderator: D. Rousset (ST-Ericsson)
16:00	**The CC-Numa TSAR Machine** H.-N. Nguyen (Bull)
16:35	**P2012 in COBRA Project: Processing Array for Computing-intensive Applications** F. Clermidy (Cea Leti)
17:00	**COMCAS Project: Energy Efficient Devices for Digital Entertainment** A. Castillejo (ST-Ericsson)
17:25	**Q&A** D. Rousset (ST-Ericsson)
	Panel Moderator: B. Candaele (Thales)
17:30	**Network on Chip - Alternative Solutions and Future Directions** C. Plomion (Arteris) P. Bricaud (Synopsys) M. Coppola (STMicroelectronics) F. Clermidy (Cea Leti) I. O'Connor (Ecole Centrale de Lyon)
18:30	**Break**
	Conference Dinner
19:30	Meeting point at hotel reception
19:45	Arrival at „Altmarktkeller" (Altmarkt 4, 01067 Dresden)
20:00	**Dinner**
23:00	End of 1st day

Wednesday, May 11, 2011

	Keynote Moderator: W. Rosenstiel (edacentrum)
9:00	**Gaining 10x in Power Efficiency in the Next Decade in Consumer Products** G. Teepe (GLOBALFOUNDRIES), P. Magarshack (STMicroelectronics)
10:00	**Coffee Break**
	Technical Session: High Level AMS Design Moderator: S. Scotti (STMicroelectronics)
10:15	**Design Refinement of Embedded Analogue and Mixed-Signal Systems** S. Scotti (STMicroelectronics), M Barnasconi (NXP), M.-M. Louerat (UPMC Paris), E. Vaumorin (Magillem)
10:50	**A Performance Comparison Between the SystemC-AMS Models of Computation** F. Paugnat, L. Bousquet, K. Morin-Allory, L. Fesquet (TIMA Laboratory)
11:15	**Virtual Prototype of a Fibre-optical Gyrosensor with SystemC-AMS** S. Rieke, O. Waydhas (Northrop Grumman LITEF)
11:40	**Q&A** S. Scotti (STMicroelectronics)
	Poster Session Moderator: R. Popp (edacentrum)
11:45	**Introduction the Poster Exhibition** Comprising accepted scientific contributions (for details see bottom of next page) and an overview on project posters and demonstrations
	Poster Exhibition
12:00	For some information on the scientific posters see bottom of next page.
12:30	**Lunch and Poster Exhibition**
	Technical Session: Design for Yield and Reliability Moderator: G. Georgakos (Infineon)
14:00	**Design Methods to Influence SoC Quality, a Post HONEY View** G. Georgakos (Infineon)
14:35	**Efficient and Reliable Feeding of the EDA Flow with Process Data** R. Gonella (STMicroelectronics)
15:00	**Methodology for Experimental Investigation of Matching and Ageing Effects** B. Dimov (IMMS), E. Hennig (IMMS)
15:25	**Q&A** G. Georgakos (Infineon)
15:30	**Coffee Break**
	Panel Moderator: D. Friebel (Fraunhofer IIS)
16:00	**More than Moore – the Most Important Driver of Microelectronics! Or?** H.-J. Brand (GLOBALFOUNDRIES) V. Herbig (X-FAB) T. Hötzel (Atmel) NN (STMicroelectronics) S. Kroehnert (Nanium) P. Schneider (Fraunhofer IIS) W. Stronski (Cadence)
17:30	**Break**
	Social Event
18:00	Meeting point at hotel reception for guided tour
18:15	Guided tour at „Deutsche Hygiene-Museum“ (Lingnerplatz 1, 01069 Dresden)
19:00	Meeting point at hotel reception
19:15	Arrival at „Deutsche Hygiene-Museum“ (Lingnerplatz 1, 01069 Dresden)
19:30	**Award of „EDA-Medaille 2011“** W. Rosenstiel (edacentrum)
19:45	**Dinner**
23:00	End of 2nd day

Thursday, May 12, 2011

	Keynote Moderator: U.Schlichtmann (TU München)
9:00	**Design and Verification of Dependable Analog Systems** L. Hedrich (U Frankfurt)
9:45	**Coffee Break**
	Technical Session: Robust Design Moderator: C. Sebeke (Bosch)
10:15	**Design Methods for ROBUST Electronic Systems - Searching for the Holy Grail?** V. Schöber (edacentrum)
10:50	**An NBTI Model for Efficient Transient Simulation of Analogue Circuits** F. Salfelder, L. Hedrich (U Frankfurt)
11:15	**Error Prediction Based on Concurrent Self-test and Reduced Slack Time** V. Gherman, J. Massas, S. Evain, S. Chevobbe, Y. Bonhomme (CEA LIST)
11:40	**Award of "EDA Achievement Award 2011"**
	Poster Exhibition
12:00	For some information on the scientific posters see below.
13:00	**Lunch and Poster Exhibition**
	Technical Session: Analog Synthesis and Optimization and 3D-Circuits Moderator: L. Hedrich (U Frankfurt)
14:15	**SyEnA Drives Synthesis-Supported Design of Analog Circuits** A. Graupner (ZMDi)
14:50	**Reliability Optimization of Analog Circuits with Aged Sizing Rules and Area Trade-off** X. Pan, H. Graeb (TU München)
15:15	**3D Physical Design: Challenges and Solutions** R. Fischbach, J. Lienig, T. Meister (TU Dresden)
15:40	**Closing** J. Haase (edacentrum)
15:50	End of 3rd day

Poster Exhibition

Within the Poster Exhibition we will have posters concerning the following scientific contributions:

A Methodology to Use Classical IP Blocks in 3D Circuits
J. Knechtel, J. Lienig (TU Dresden)

Robustness Evaluation of Embedded Software Systems
W. Lu (U Stuttgart), M. Metzdorf, D. Helms (OFFIS), M. Radetzki (U Stuttgart), W. Nebel (OFFIS)

Shared-memory Communication in Distributed SoCs on Multi-FPGA Systems
M. Müller, O. Brandel, W. Fengler (TU Ilmenau)

Fully Coupled Circuit and Device Simulation with Exploitation of Algebraic Multigrid Linear Solvers
B. Klaassen, T. Clees, M. Selva Soto (Fraunhofer SCAI), C. Tischendorf (U Köln)

Impact Estimation for Design Flow Changes
R. Koppe, S. Häusler, F. Poppen (OFFIS), A. Hahn (U Oldenburg)

Besides these reviewed contributions to edaWorkshop11, the poster exhibition will show posters and demonstrations of all EDA projects funded by BMBF within IKT 2020.

Program

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Location

Dresden, the capital of Saxony and the former residence of the Wettin dynasty, is a city of art and culture with magnificent buildings, many world-class museums as well as a rich tradition of theatre and music. No book about the history of architecture can forget to mention Dresden's Zwinger Palace. The reconstructed Frauenkirche, the Semper Opera House and the Royal Palace as well as many other historical monuments and collections define the image of the city.

See also: www.dresden.de

The event takes place at the 4-star Dorint Hotel Dresden which is located close to the Old Town. For attendees of the eda-Workshop11 and CATRENE DTC edacentrum has arranged special room rates, valid from May 9 – 12, 2011.

Please book your room by April 10, 2011, and mention "edaWorkshop11" as the keyword. After April 10, the fixed quota of rooms for the event will be closed. All participants are kindly asked to make their own hotel reservations directly:

Dorint Hotel Dresden
Grunaer Straße 14
01069 Dresden
Germany

Fon +49 351 4915-0
Fax +49 351 4915-100
www.dorint.com/en/hotel-dresden

Special Room Rates at Event Hotel				
Dorint Hotel Dresden	Single room	EUR 110,–	incl. breakfast	Fon +49 351 4915-774
	Double room	EUR 140,–	incl. breakfast	anke.boehmer@dorint.com

For alternative hotels see www.edacentrum.de/edaworkshop/location

Directions to the Dorint Hotel Dresden

From the airport
By taxi:
The taxi fare to the hotel is about EUR 18.

By public transportation:
Take S2 local train (direction "Heidenau"), get off at "Dresden Hauptbahnhof". See description from the main railway station.

See also:
www.dresden-airport.de

From the main railway station
Take tram no. 3 (direction "Dresden Wilder Mann") or 7 (direction "Weixdorf"), get off at "Pirnaischer Platz". Take tram 2 (direction "Dresden Kleinzschachwitz Freystraße") or 12 (direction "Dresden Ludwig-Hartmann-Straße"), get off at "Deutsches Hygiene-Museum". Or walk along the "Grunaer Straße" from "Pirnaischer Platz" in about 9 minutes

See also: www.dvb.de

From the west via A4/A14 (Frankfurt/M, München, Leipzig)
Exit no. 77b "Dreieck Dresden West" into motorway A17 (direction Prag), take exit no. 3 "Dresden Südvorstadt" into B170 towards "Dresden Zentrum" (approximately 6 km), drive straight ahead up to "Pirnaischer Platz", turn right into "Grunaer Strasse" (direction "Gruna"), after 200 m the Dorint Hotel is on the right side.

From the north/east via A4/A13 (Hamburg, Berlin, Bautzen)
Exit Nr. 81a "Dresden/Hellerau" into B170 towards "Dresden Zentrum" (approximately 7 km), pass the bridge "Carolabrücke", at the 2nd crossroad at "Pirnaischer Platz" turn left into "Grunaer Strasse" (direction "Gruna"), after 200 m the Dorint Hotel is on the right side.

Using a navigation system
Choose "Pirnaische Vorstadt" as district when you enter "Grunaer Strasse".