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Panel Level Packaging Consortium Moving to the Next Level

Mobile consumer electronics and driverless cars are powering a new wave of developments in electronic packaging. Berlin's Fraunhofer IZM is the place to be for leading industry enterprises wishing to develop the fundamental processes for new panel-level packaging and creating viable first demonstrators on large-scale organic substrate formats. After the successful conclusion of its two-year venture, the consortium is embracing new members and exciting new research avenues. The institute is speaking to private enterprises from around the globe to take the results from the first consortium to the next level with the industry leaders in production technology and materials development.

The Fraunhofer Institute of Reliability and Microintegration IZM is a renowned expert for wafer-level packaging and substrate technologies. This expertise made it the natural seedbed for a high-powered project with 17 dedicated partners from industry: The Panel-Level Packaging Consortium. The international consortium has created the foundations for novel process that allow the production of low-cost packages on full-panel formats (18 x 24 inch) on an industrial scale. It has developed extremely thin components that forego the usual substrate without compromising on their excellent electrical properties and remarkably low thermal resistance. The short electrical connections made possible in this manner makes the resulting packages an ideal choice for high-frequency applications like 5G or radar technologies (with great potential e.g. for driverless cars). The focus of the consortium's two years of hard work was the process chain in panel-level packaging: from assembly, molding, wiring, cost modelling, and standardization.

The unexpected success of the venture has motivated Fraunhofer IZM to launch a second consortium of its kind: the all-new PLC 2.0. Many of the actors from the consortium's first incarnation will return, but new members are explicitly welcomed. Moving beyond the rather general goals of the first consortium, the returning members and their new partners will concentrate on three specific avenues to pursue: first, they are refining and fine-tuning the technological innovations, especially in terms of the interfaces between each process step. Next, they are working on pushing the scale of the wire connections to the limits of miniaturization, an inevitable effort, as the increasingly minute struc-tures on the chip level demand higher-density wiring on organic substrates. The PLC 2.0 consortium has set itself the challenging goal of achieving 2 µm width at 2 µm distance without affecting the reliability of the systems, making electromigration and copper diffusion key objects for their coming research efforts. On a less technical level, the consortium's work will be rounded off with an expansion of the original cost model.

Fraunhofer IZM installed new facilities in the run-up to the PLC 2.0 to prepare for these challenges, benefitting from the support of the German Federal Ministry of Education and Research in the form of several of the major investments coming as part of the Research Fab Microelectronics Germany. The successful implementation of the workflow allowed a simplification of the consortium's structure to a single member-ship category. Tanja Braun, public face of the Panel Level Consortium and Group Lead at Fraunhofer IZM, has reason to be optimistic: "We are planning to put the new consortium into action in December 2019, and I am already excited to see which companies will come and join us as we push ahead to the next level."

300000 Chips, 30000 SMDs, and 110 panels in 2 years

The track record of the first consortium speaks volumes: In the first year alone, the entire process chain from assembly to forming and separation was established and optimized for semi-format panels (18 x 12 inch), with dedicated testing procedures and demonstrators for use in initial reliability tests. The consortium committed its second year to the modification of this original design, scaling the technology to full-format panels (18 x 24 inch) on the basis of the first year's findings and integrating new vertical integration elements and passive components. In total, more than 110 panels were produced in these two years, including almost 300000 chips and 30000 SMDs. Progress was not limited to the technology alone, as the consortium also produced a comprehensive, but sufficiently flexible cost model to cover different types of applications and materials. The output of these research efforts was shared with the wider public at numerous scientific conferences and industry expos.

Tanja Braun and Michael Töpper raised the issue of standardized panel sizes at several public events, fueling a standardization initiative as part of SEMI that many of the PLC members contributed to. The PLC 1.0 is rightly considered one of the top ventures in its area. The success of the consortium was made possible by the work of Fraunhofer IZM and its partners: the Ajinomoto Group, Amkor Technology, ASM Pacific Technology Ltd., Atotech Deutschland GmbH, Österreich Technologie & Sys-temtechnik AG, Brewer Science, Inc., Evatec AG, FUJIFILM Electronic Materials USA, Hitachi Chemical Company Ltd., Intel Corporation, Meltex Inc., Merck KGaA, Mitsui Chemicals Tohcello, Semsysco GmbH, ShinEtsu Chemical, SÜSS MicroTec SE, and the Unimicron Technology Corp.

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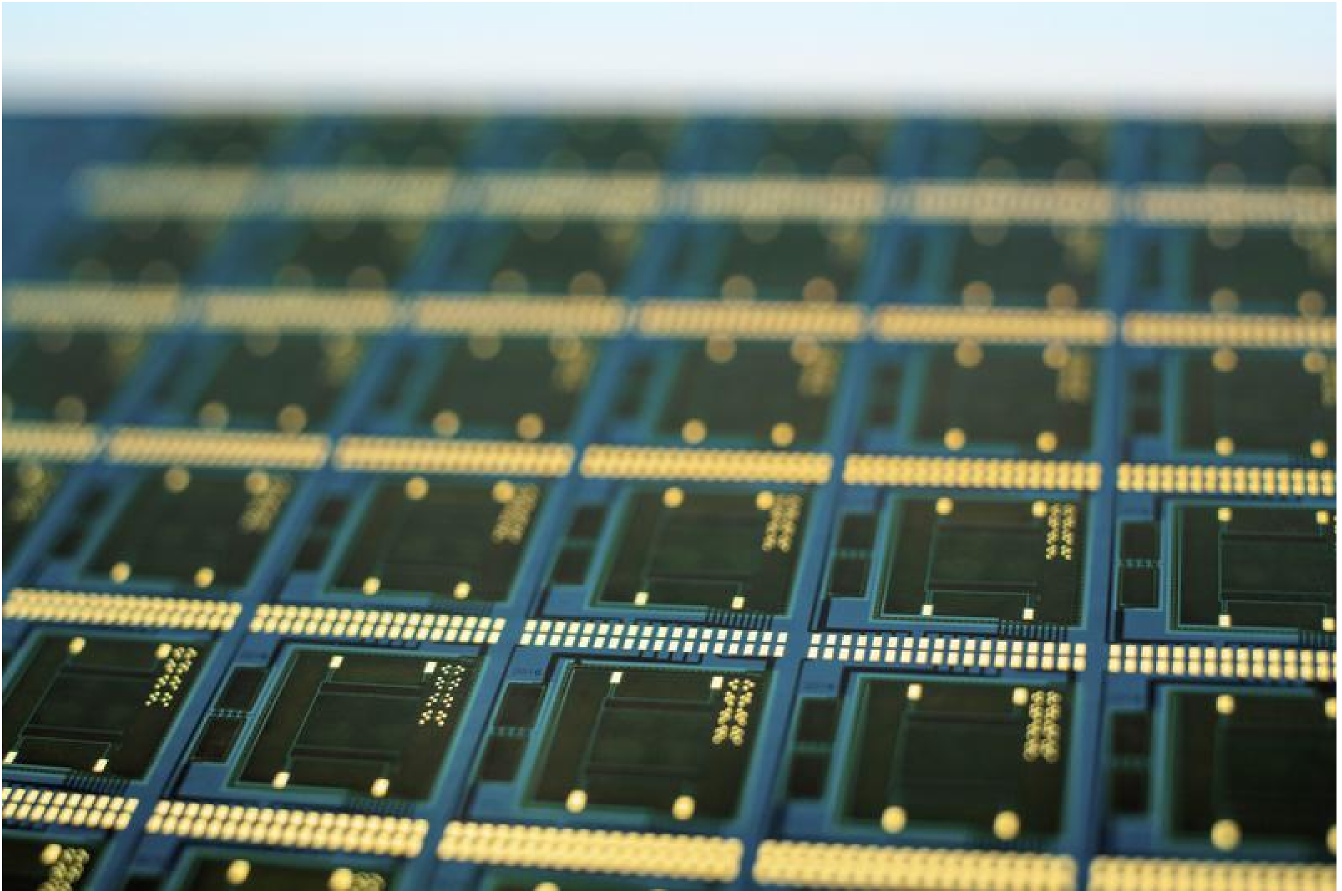

PLP 2.0 had been set up to further advance the technological development of industrially applicable processes for the manufacture of low-cost packages using the panel format.
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